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POWER ELECTRONICS & MOTION CONTROL

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SUBMITTED TO

PROF.

TERM PROJECT

DESIGNING AND BUILDING A BUCK CONVERTER

PROJECT REPORT

STUDENT ID	NAME -SURNAME

SUBMISSION DATE:

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1. Purpose of the Project

The main goal of the project is to design and built a DC/DC Buck Converter.

2. Introduction

The step-down dc–dc converter, commonly known as a buck converter, consists of dc input voltage source *VS*, controlled switch S, diode D, filter inductor *L*, filter capacitor *C*, and load resistance *R*. Typical waveforms in the converter are shown in Figure 2 under assumption that the inductor current is always positive (CCM). The state of the converter in which the inductor current is never zero for any period of time is called the continuous conduction mode (CCM). It can be seen from the circuit that when the switch S is commanded to the *on* state, the diode D is reverse biased. When the switch S is off, the diode conducts to support an uninterrupted current in the inductor. The relationship among the input voltage, output voltage, and the switch duty ratio *D* can be derived, for instance, from the inductor voltage *vL* waveform (see Fig. 13.4b). According to Faraday's law, the inductor volt–second product over a period of steady-state operation is zero.

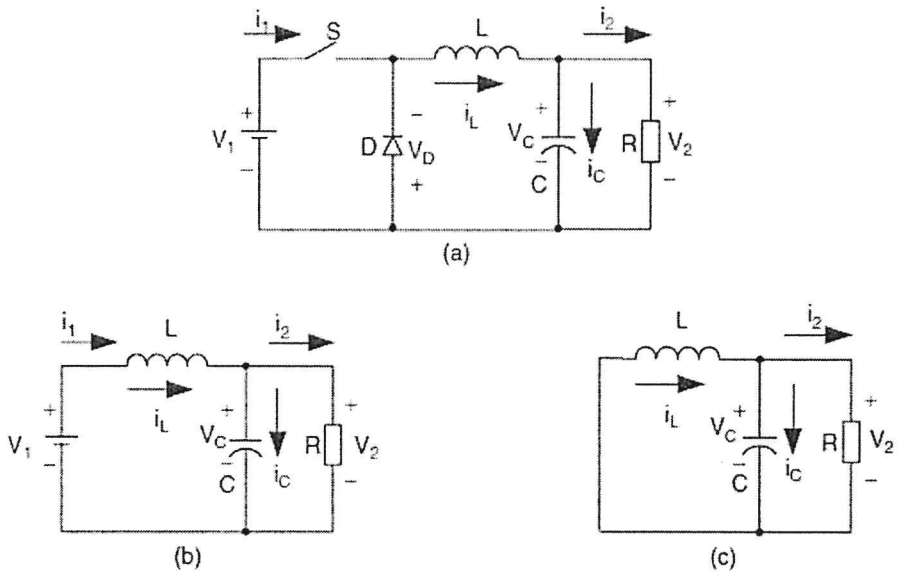


Figure 1. Simple circuit scheme of a buck converter: (a) circuit diagram; (b) switch-on equivalent circuit; and (c) switch-off equivalent circuit [1].

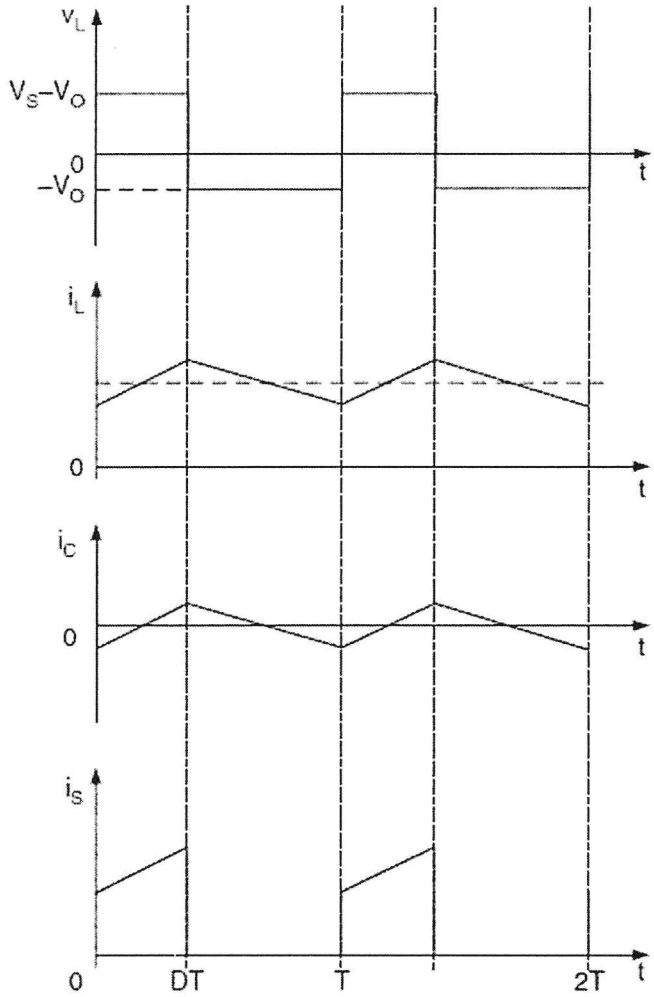


Figure 2. Voltage-current waveforms for buck converter in CCM mode [1].

3. Designing and Building a DC/DC Buck Converter

The input and output parameters are given below. Output current must be equal to or higher than 4A. Maximum – minimum voltage parameters are from 5V to 45V. According to the requirements,

$V_{in} = 24V$.

$V_{out} = 12V$ decided.

Duty ratio

$$D = \frac{V_{out}}{V_{in}} = \frac{12}{24} = 0.5$$

Output current for a resistive load is decided as

$I_R = I_L = 4A$

The process of the project, so the selection of the circuit elements can be examined in several stages. Corresponding statements about PWM Controller Part, Gate Driver Part and the Power Stage Part is given further.

3.1.PWM Controller Part:

Acquiring and controlling the square waveform and then driving the MOSFET are the main parts of the design. SG3525A is used as a PWM Controller. SG3525A is a pulse width modulated integrated circuit, designed to offer higher performance and lower external parts and to be used in power switching applications. The pinout scheme is given in Figure 6. Required circuit elements R_T, R_D, C_T are used to set the oscillation frequency. Here, R_T is the timing resistor that adjusts the oscillator frequency. R_D is the discharge resistor and C_T is the timing capacitor. Frequency of the saw-tooth waveform can be calculated from

$f = \frac{1}{C_T(0.7R_T+R_D)} = 100kHz$ decided.

The essential values of R_T, R_D, C_T are decided with reference to the oscillator charge time and oscillator discharge time graphics, given in figures 7 and 8. Also, at this point, pins 5, 6 and 7 are used according to the given connection diagram in the project and in the UC3525A datasheet.

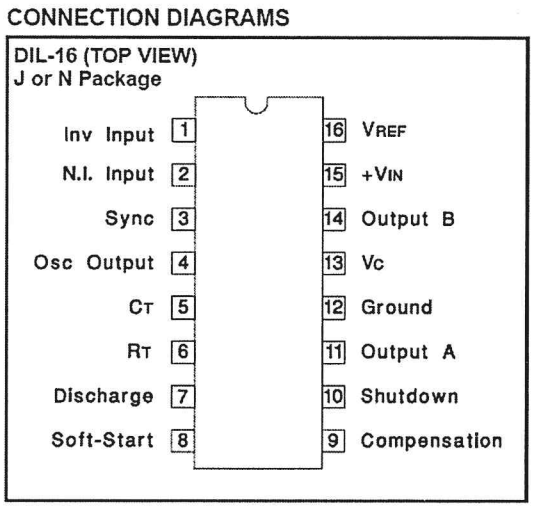
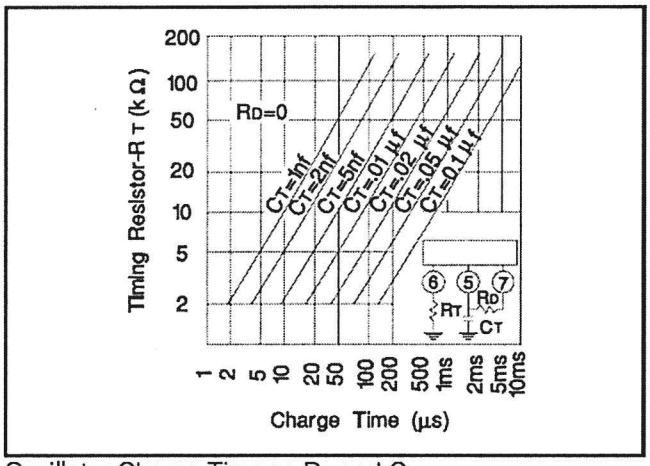


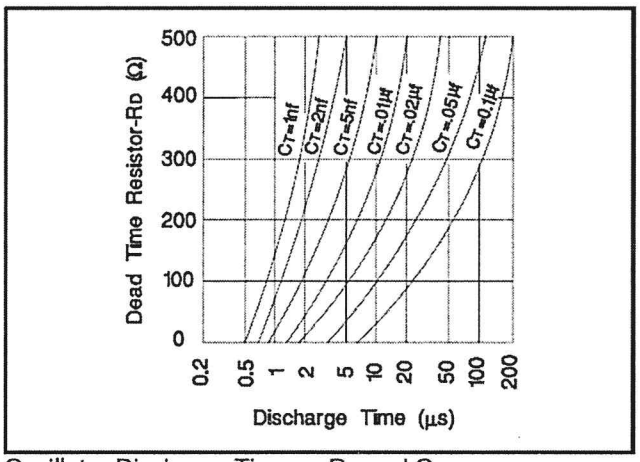
Figure 3. Connection diagram of UC3525 [2]

Oscillation frequency of the MOSFET is given as $f_s = 100kHz$. So the charge time can be calculated as 10 μs. Discharge time of the capacitor C_T is dreadfully small unlike the charge time due to the saw-tooth waveform. As the dead time resistor is chosen as 0Ω, 2nF timing capacitor C_T is extremely enough. Here, timing resistor is calculated as $R_T = 7k\Omega$. From the Figure 7, timing resistor can be chosen 5KΩ potentiometer with considering adjusting the oscillation frequency.



Oscillator Charge Time vs R_T and C_T.

Figure 4. Oscillator charge time graphic as a function of resistor R_T and capacitor C_T [2].



Oscillator Discharge Time vs R_D and C_T.

Figure 5. Oscillator discharge time graphic as a function of resistor R_D and capacitor C_T [2].

Absorbing the AC part of the output voltage at the reference regulator is ensured by using 0.1uf valued capacitor C_3. Thus; across the 10KΩ valued potentiometer R_2, DC voltage occurs. The value of R_2 is decided with reference to laboratory test figure in the SG3525A datasheet. It is also considered that, R_2 potentiometer should be capable of adjusting the duty cycle to change the output voltage. It could be elaborated in this way: There is an internally

well-regulated +5.1V voltage in the pin16 inside the 3525. So, reference voltage of the error amplifier can be set. According to connection way of the pins 2 and 9, as the duty cycle adjusted by changing the position of R_2 potentiometer, voltage comparator at pin9 can perceive the amplitudes of $V_{C_3}$and V_{R_2}. When $V_{R_2}$is greater than V_{C_3}, outputs of the chip are high in alternated period, conversely the outputs of the chip are zero.

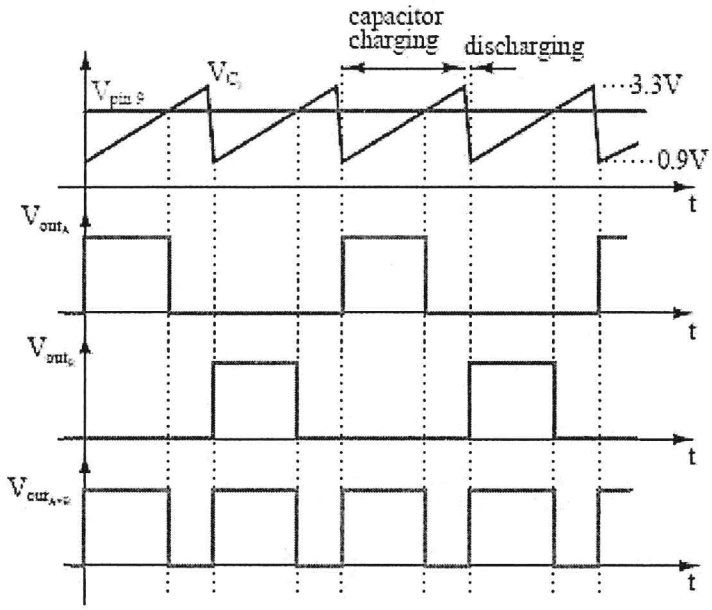
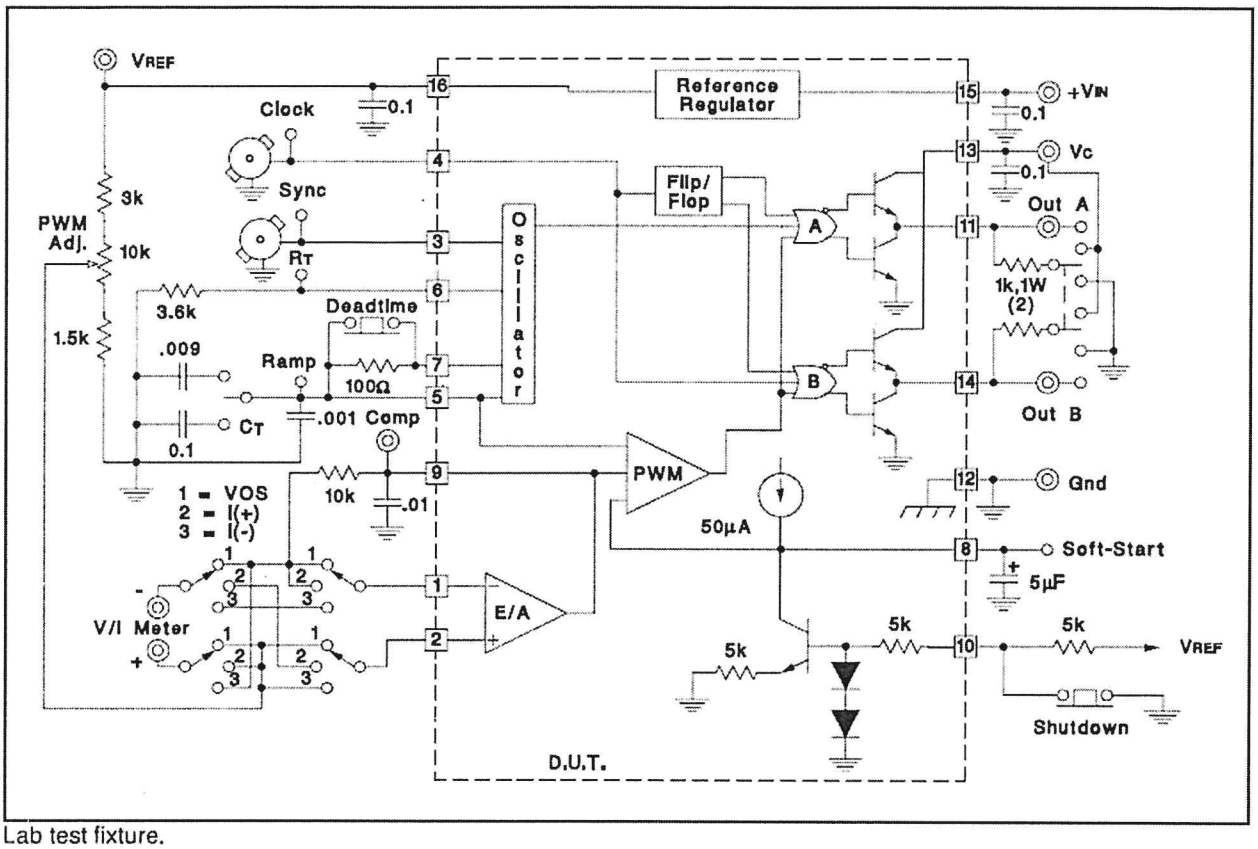


Figure 6. SG3525A Comparator input-output waveforms [2].

The values of the output resistors R_4, R_5 and softstart capacitor C_2 soft-start capacitor are decided according to the SG3525A datasheet. R_4, R_5 are 1KΩ, 1W and C_2 is 5uf. Here, the value of C_2 states the response time of R_2 potentiometer.

For closed-loop operation, a reference signal which is obtained by the voltage divider resistors 7.5kΩ at the output, is sent to the compensation pin of UC3525A and the inv. input pin.



Lab test fixture.

Figure 7. Connection Diagram of the controller SG3525A lab test figure [1].

3.2.Gate Driver Part:

The output current of SG3525A is about 100mA and is not enough to charge the capacitor at the gate of the MOSFET in required frequency. So, a non-inverting gate driver chip TC427 is used to resolve difficulty. . Output signal of 3525 is not enough to drive the MOSFET. Peak output current of TC427 is 1.5A. This value is high enough to charge and discharge the capacitor at the MOSFET's gate. Related functional block diagram is given in Figure 9.

Pinout scheme of TC427 with the functional block diagram is given below.

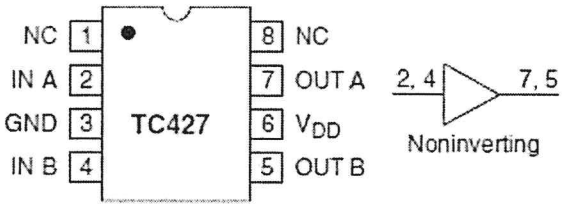


Figure 8. Pinout scheme of TC427 IC [3].

Capacitors C_4, C_5, C_6 and C_7 are used for decoupling. The values of C_4, C_5, C_6 are 0.1uf with ceramic type, C_7 is 33uf with electrolytic type. All of the mentioned values are determined due to the TC427 datasheet.

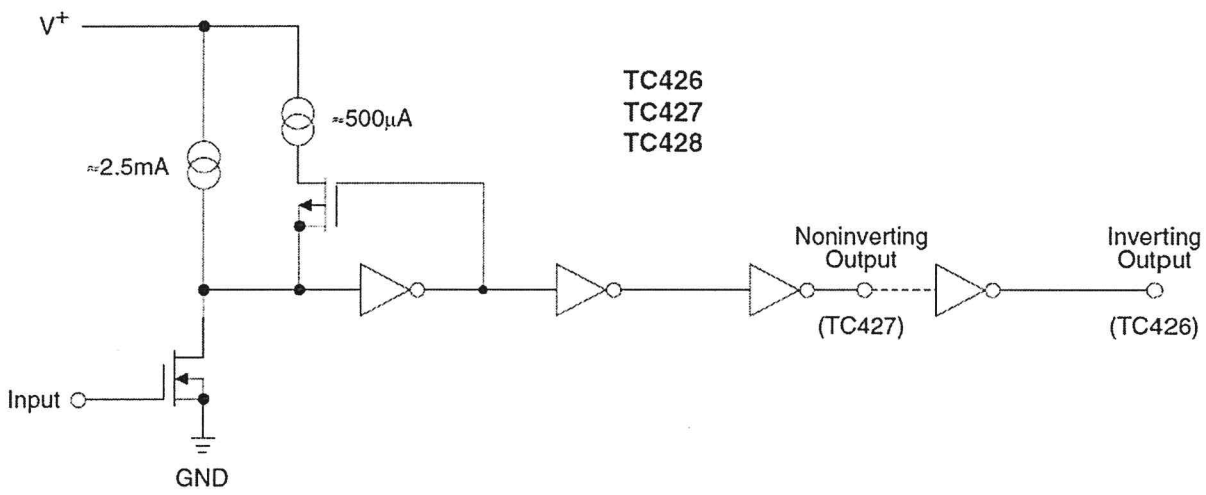


Figure 9. Functional block diagram of TC427 IC [3].

A 10Ω resistor R_g is used at the output of the TC427. The reason is to limit the oscillations that may occur in the PWM waveform. This condition is risky and can be harmful for MOSFET, if the amplitude of oscillations is greater than MOSFET's breakdown voltage $V_{bd} = 20V$. Limiting the gate-source voltage is vital to protect the MOSFET. Thus, gate drive voltage also must be bounded at about 18V. Zener diodes D_1 and D_2 with $V_{bd} = 18V$ breakdown voltage and diodes D_3, D_4 for preventing the zener diodes from positive anode to cathode voltage are used.

7812 Voltage regulator is also used to supply the integrated circuits SG3525A and TC427.

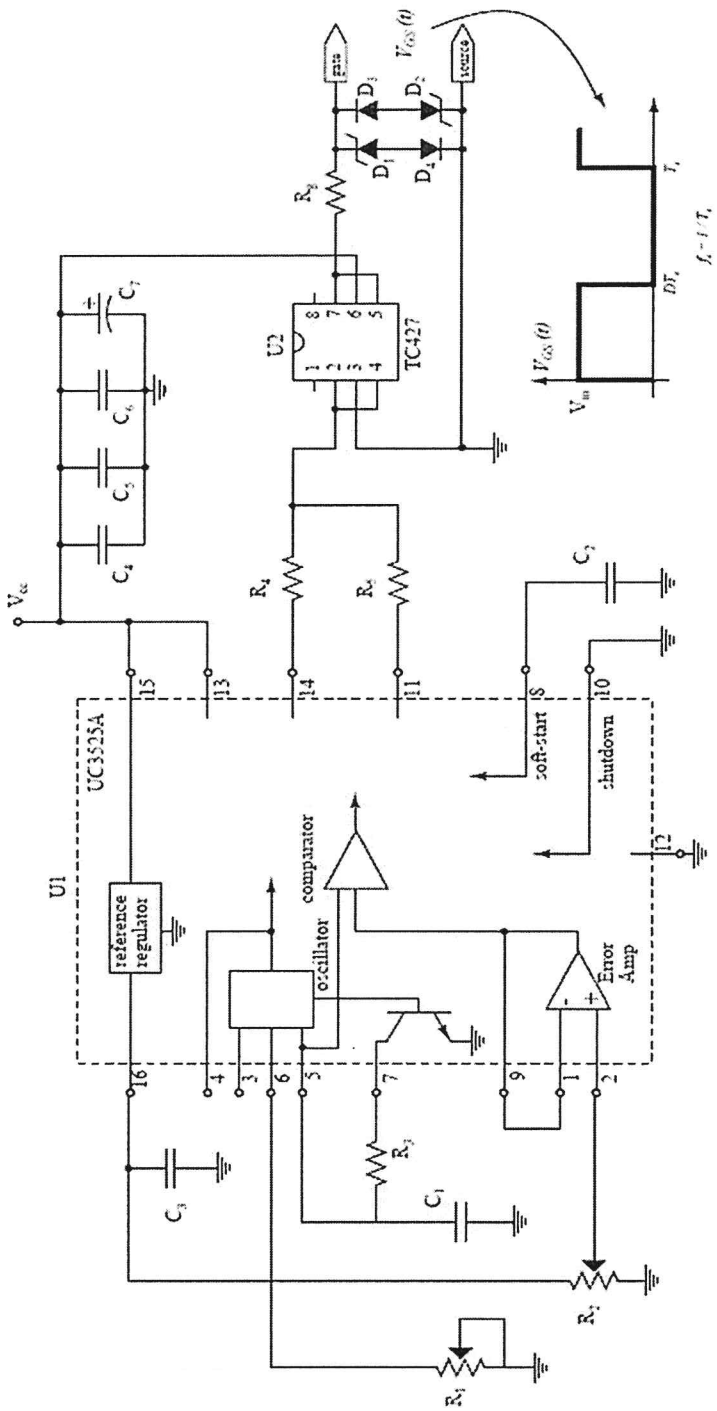


Figure 10. Controller part connection diagram [2].

3.3. Power Part:

3.3.1. MOSFET Switch

IRF3205 is used as power MOSFET for switching in the power stage part. Specific electrical characteristics are given further according to the datasheet; $V_{gs} = \pm 20V$, $V_{ds} = 55V$, $I_d = 110A$. As seen from the parameters, MOSFET is adequate for high current and high frequency applications.

Switching Loss of IRF3205

Required parameters, which is used to calculate the over-all loss:

Operation parameters:

$$V_{DS} = 24V$$
$$I_D = 4A$$
$$f_s = 100kHz$$
$$D = 0.5$$

MOSFET Characteristics:

$$R_{DS(on)} = 8m\Omega$$
$$t_{d(on)} = 14ns$$
$$t_r = 101ns$$
$$t_{d(off)} = 50ns$$
$$t_f = 65$$

Switching losses during turn on,

$$t_{turn-on} = 14 + 101 = 115ns$$

$$P_{turn-on} = \frac{1}{2} \times V_{DS} \times I_D \times t_{on} \times f_s = \frac{1}{2} \times 24 \times 4 \times 115 \times 10^{-9} \times 100 \times 10^3 = 0.552W$$

Since $t_{turn-on} = t_{turn-off} = 115ns$

Turn-off losses,

$$P_{turn-off} = 0.552W$$

$$P_{switching} = P_{turn-on} + P_{turn-off} = 1.104W$$

During switch is in ON state,

$$t_{ON} = T \times D - \left(t_{d(on)} + t_r + t_{d(off)} + t_f\right) = 4.77\mu s$$

$$P_{ON} = I_D^2 \times R_{DS(on)} = 4^2 \times 8 \times 10^{-3} \times 4.77 \times 10^{-6} \times 100 \times 10^3 = 0.06W$$

During switch is in OFF state,

$t_{OFF} = T \times D = 10 \times 10^{-6} \times 0.5 = 5 \times 10^{-6}\mu s$

$P_{OFF} = V_{DS} \times I_{leakage} \times t_{ON} \times f_s = 3 \times 10^{-4}W$ can be neglected.

So, total loss of IRF3205 MOSFET is

$P_{total} = 1.104 + 0.06 = 1.164W$

3.3.1.1.Heatsink Calculations

Required thermal characteristics for IR3205 are given in the datasheet.

Table 1. Thermal resistance of IRF3205 [4].

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.75	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

www.irf.com 1

Operating junction: $-55°C < T_J < +175°C$

For periodic pulses, heatsink determination can be completed due to related equations given below.

$T_J = T_C + r(t) \times R_{JC} \times P$ (1)

$T_C = T_A + P_o \times (R_{CS} + R_{SA})$ (2)

$P_o = P \times D$ (3)

It is assumed that operating junction $T_J \approx 120°C$.

Thermal response r(t) is determined from the Figure .... Given in the datasheet. For D=0.5 at f=100kHz switching frequency, r(t)=0.65.

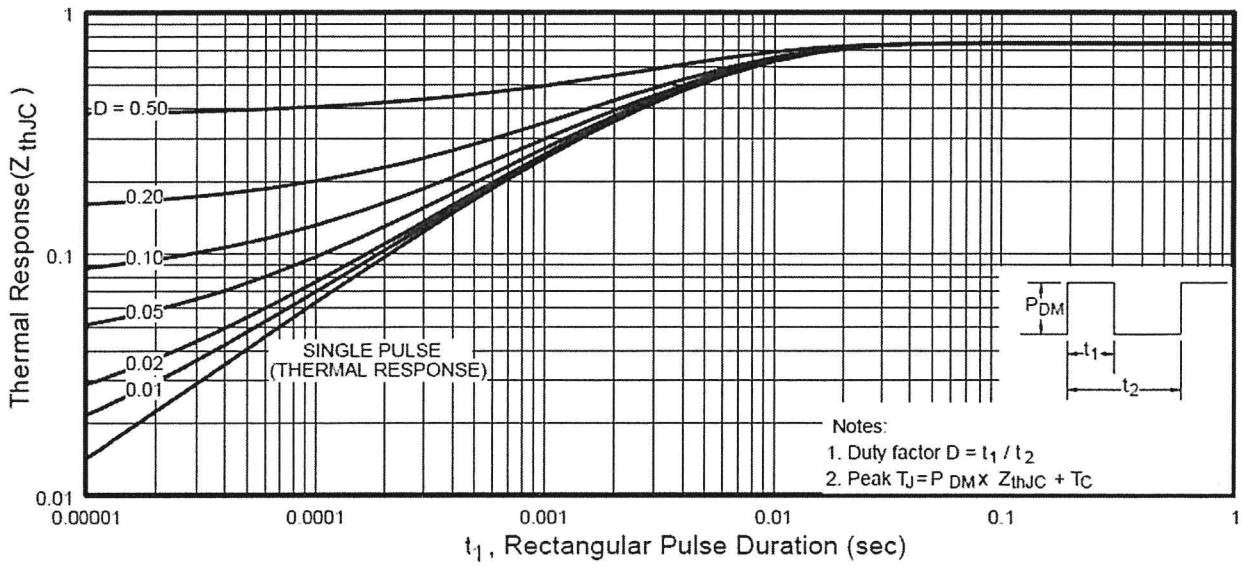


Figure 11. Thermal response of IRF3205 for different duty ratio values [4].

Power dissipation P=1.164W as calculated above.

From the equation (1)

$T_C = 119.4°C$

When the ambient is temperature is maximum 30°C decided, required sink-to-ambient resistor R_{SA} can be calculated from (2). Then heatsink dimensions and material is stated. Since it is hard to find required heatsink material in appropriate dimensions, a Standard heatsink for MOSFET is used.

3.3.1.2.RCD Snubber Calculations

Snubber circuit alters the MOSFET voltage and current waveforms to an advantage. The snubber provides another path for load current during turn-off. As the MOSFET is turning off and the voltage across it is increasing, the snubber diode $D_s$becomes forward biased and the snubber capacitor C_s begins to charge. The rate of change of MOSFET voltage is reduced by the capacitor, delaying its voltage transition from low to high. The capacitor charges to the final off-state voltage across the MOSFET and remains charged while the MOSFET is off.

When the MOSFET is on, the capacitor discharges through the snubber resistor and MOSFET.

Snubber capacitor C_s is calculated from the equation below.

$$C_s = \frac{I_L \times t_f}{2 \times V_{in}} = \frac{4 \times (65 \times 10^{-9})}{2 \times 24} = 5.42nF$$

$C_s = 10nF$ decided.

The resistor is chosen such that the capacitor is discharged before the next time MOSFET turns off. A time interval of three to five time constants is necessary for capacitor discharge.

$t_{on} > 5RC$

$R_s < \frac{t_{on}}{5C} = \frac{5 \times 10^{-6}}{5 \times 10 \times 10^{-9}} = 100\Omega$ should be chosen.

3.3.2. Diode

A fast type diode is required. When the switch condition is zero, the current across the load completes its loop from the diode. Thus, the freewheeling diode should be high current capable. Thus, 15A shottky barrier rectifier MBR1560CT is used.

3.3.3. Inductance – Capacitor (LC Low pass filter)

Calculations are completed considering the CCM (Continuous Current Mode) operation.

Here, as mentioned before

$V_{in} = 24V$.

$V_{out} = 12V$ - $I_{out} = 4A$

D=0.5

The load

$$R = \frac{V_{out}}{I_{out}} = \frac{12}{4} = 3\Omega$$

Minimum inductance value for CCM is

$$L_{min} = \frac{(1-D)\times R}{2f} = \frac{(1-0.5)\times 3}{2\times 100\times 10^3} = 7.5\mu H$$

Inductance value should be greater than the minimum. Thus, $L \cong 15\mu H$ can be selected. The maximum voltage across the switch and diode is 24V. The inductor voltage when the switch is closed is $V_{in} - V_{out} = 24 - 12 = 12V$, when the switch is open is $-V_{out} = -12V$. So, the inductor must withstand 12V.

- Core: 77310-A7 Kool Mμ Toroid type is used to obtain L=25μH at f=100kHz operating frequency.

$$\Delta i_{L,closed} = \frac{(V_{in}-V_o)}{L} D.T = 6A$$

$$\Delta i_{L,closed} = -\frac{-V_o}{L}(1-D).T = -6A$$

$$I_{max} = I_L + \frac{\Delta i_L}{2} = 7A$$

$$I_{min} = I_L - \frac{\Delta i_L}{2} = 1A$$

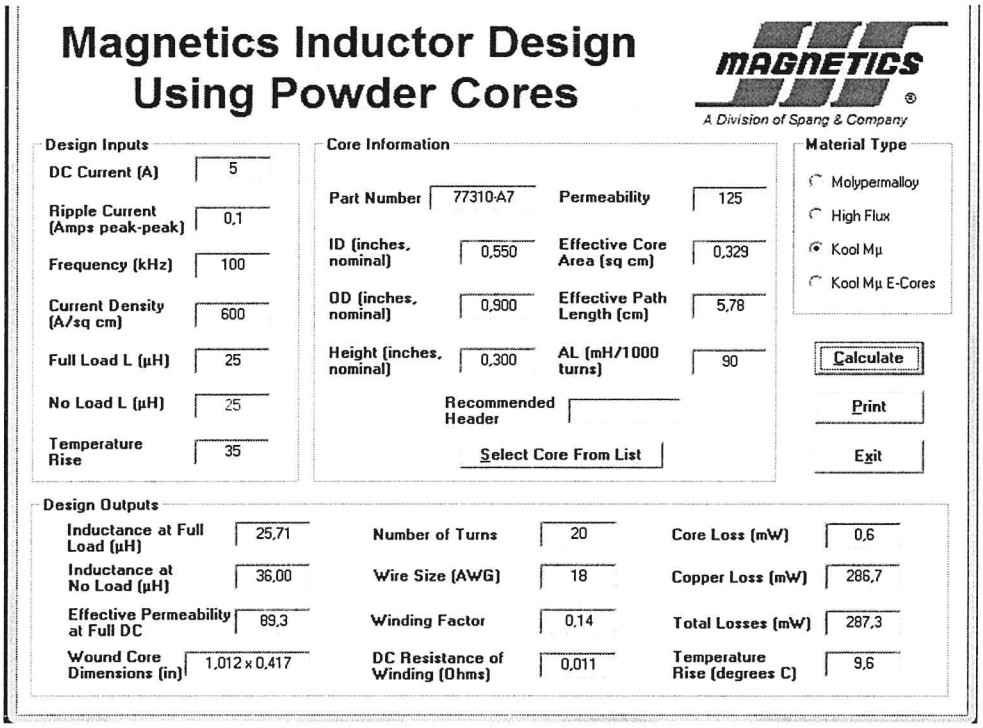


Figure 12. Magnetics Inc. Inductor design program for core determination.

Voltage ripple is decided

$$\frac{\Delta V_o}{V_o} = \%0.5$$

$$\frac{\Delta V_o}{V_o} = \frac{(1-D)}{8.L.C.f^2}$$

From the equation Capacitor value is calculated

$$C = 125\mu F$$

Capacitor must be rated for the 12V output.

Selected component values are simulated in PSIM before construction and testing. Settling time and ripple voltage parameters are observed for different LC values. For L=25µH and C=100µF, the adequate waveforms are stated.

4. Simulation:

PSIM is used for the simulation phase.. In simulation, in order to produce the square wave form, gate block is applied instead of SG3525A.

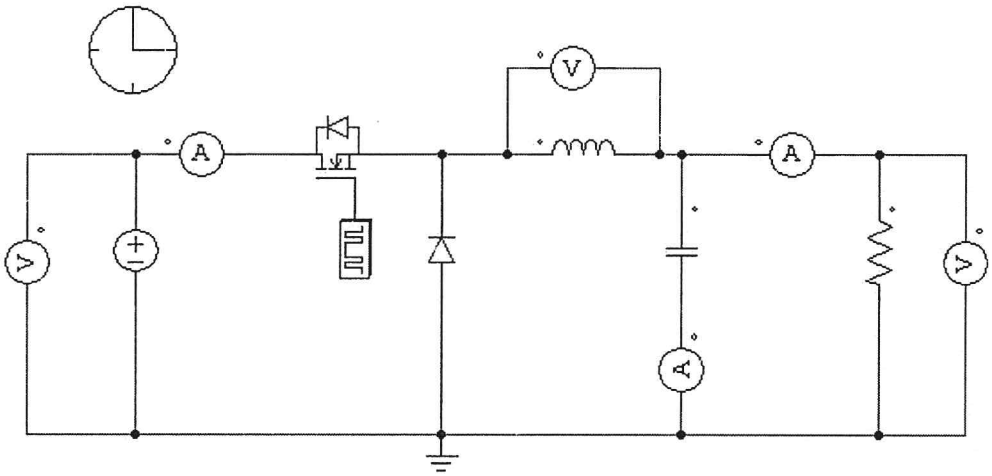


Figure 13. Simulated diagram of the circuit in PSIM.

All the graphics that are obtained by the simulation are in continuous current mode. During the simulation, set time of the system is observed by varying the L-C values. For the calculated values, peak voltage – current parameters are higher and set time is longer. After the simulation for $L = 25\mu H$ and $C = 25\mu F$ appropriate waveforms are obtained.

Simulation phase is also repeated for the closed – loop operation. Required waveforms at f=100kHz frequency and D=0.5 are given below.

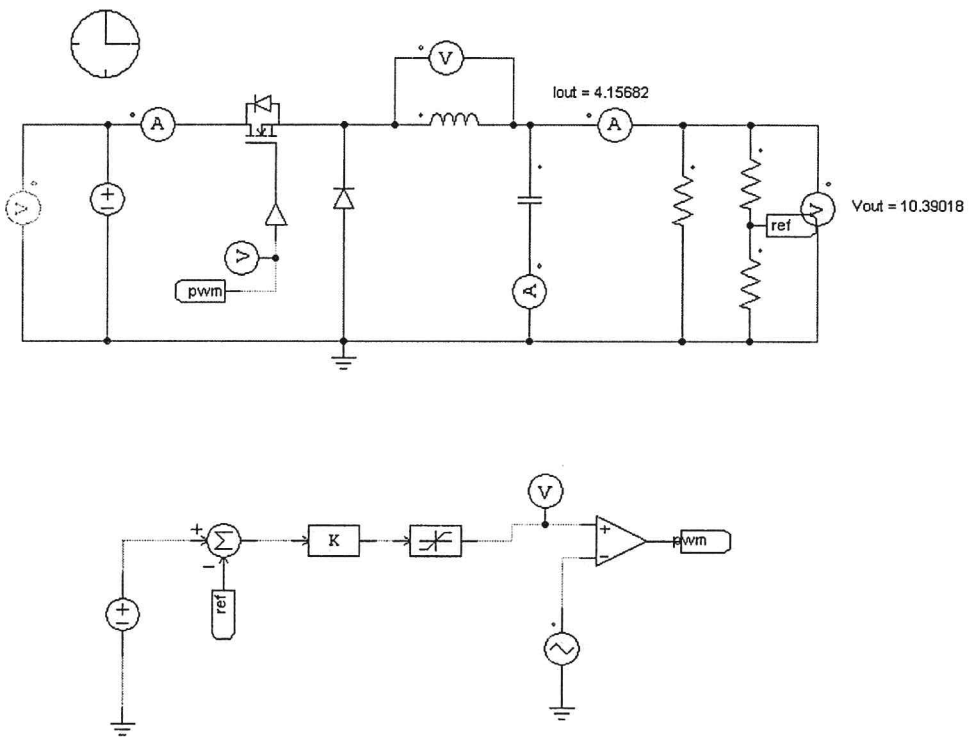


Figure 14. Simulated circuit scheme for cloased loop operation.

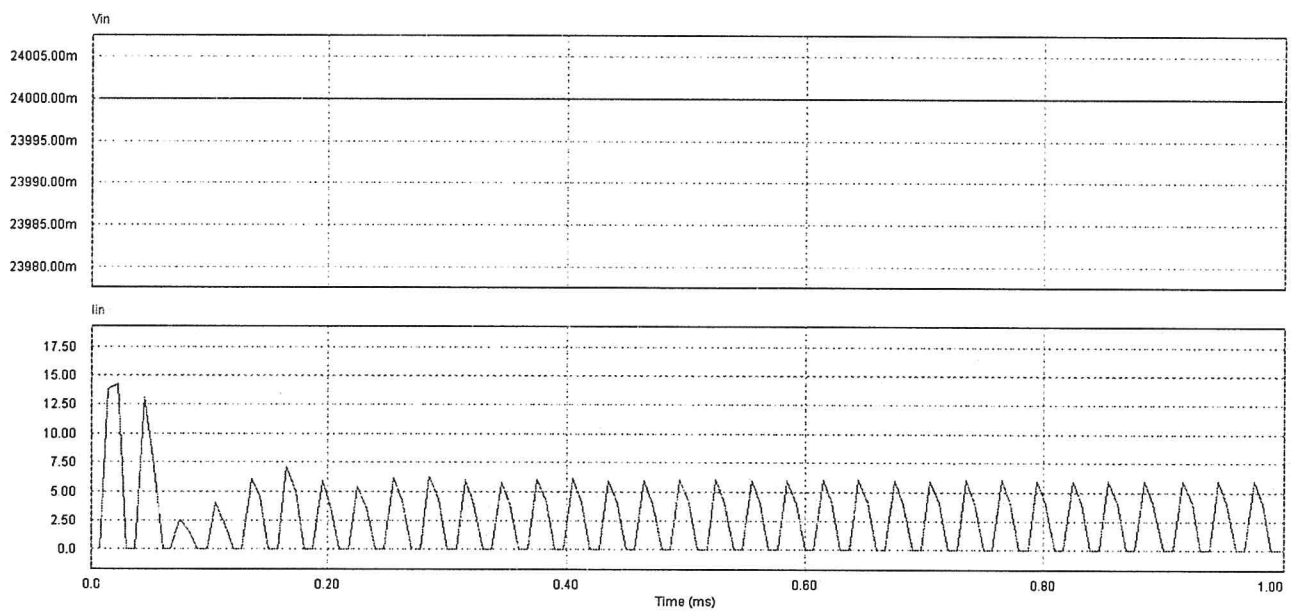


Figure 15. Input Voltage – Current waveforms.

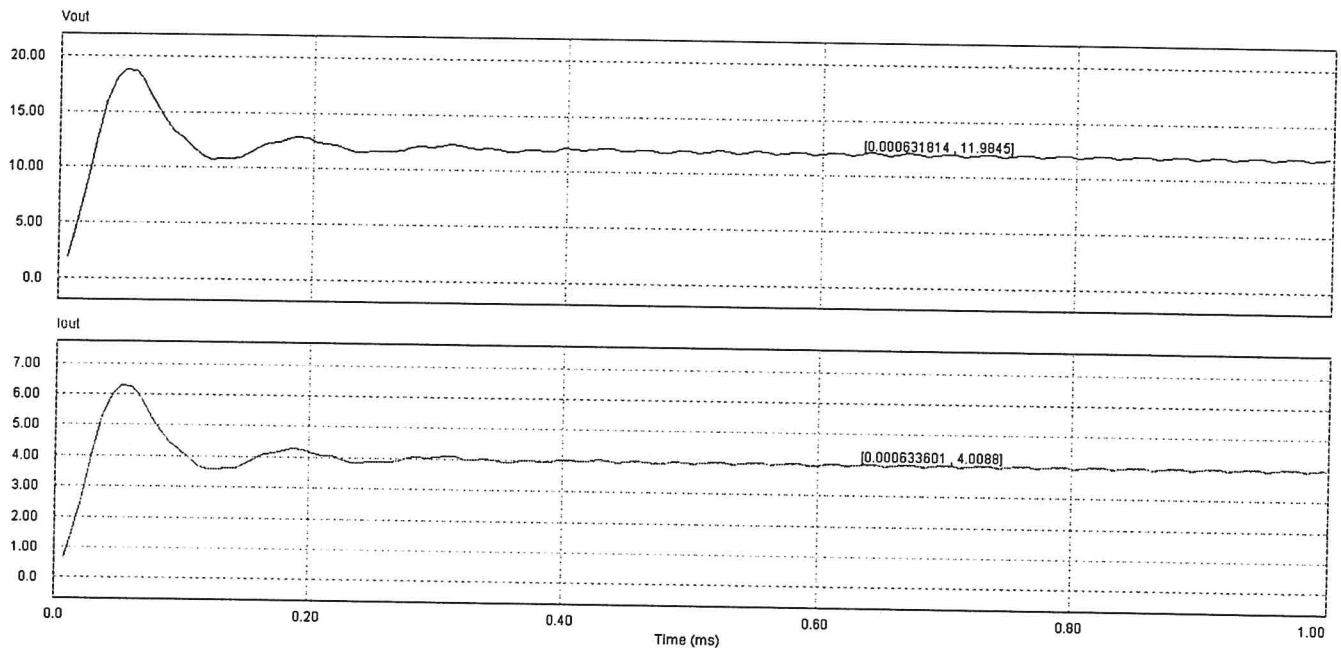


Figure 16. Output Voltage – Current waveforms.

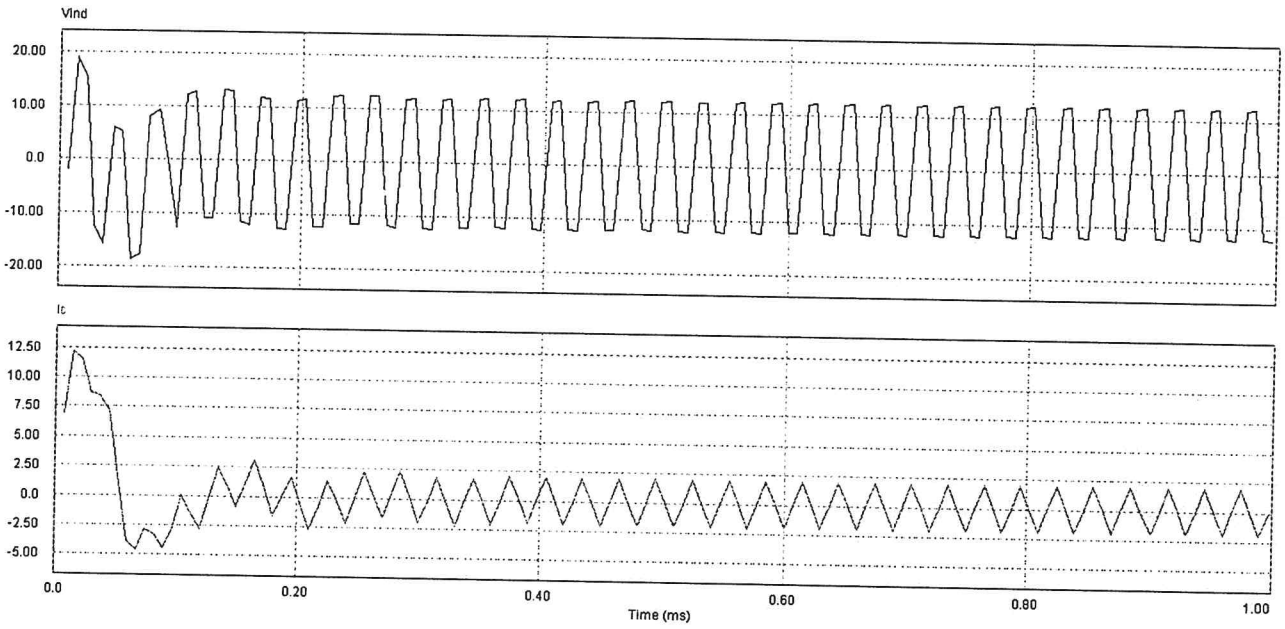


Figure 17. Inductor voltage and capacitor current waveforms.

5. Construction and Testing

5.1. Breadboarding Phase:

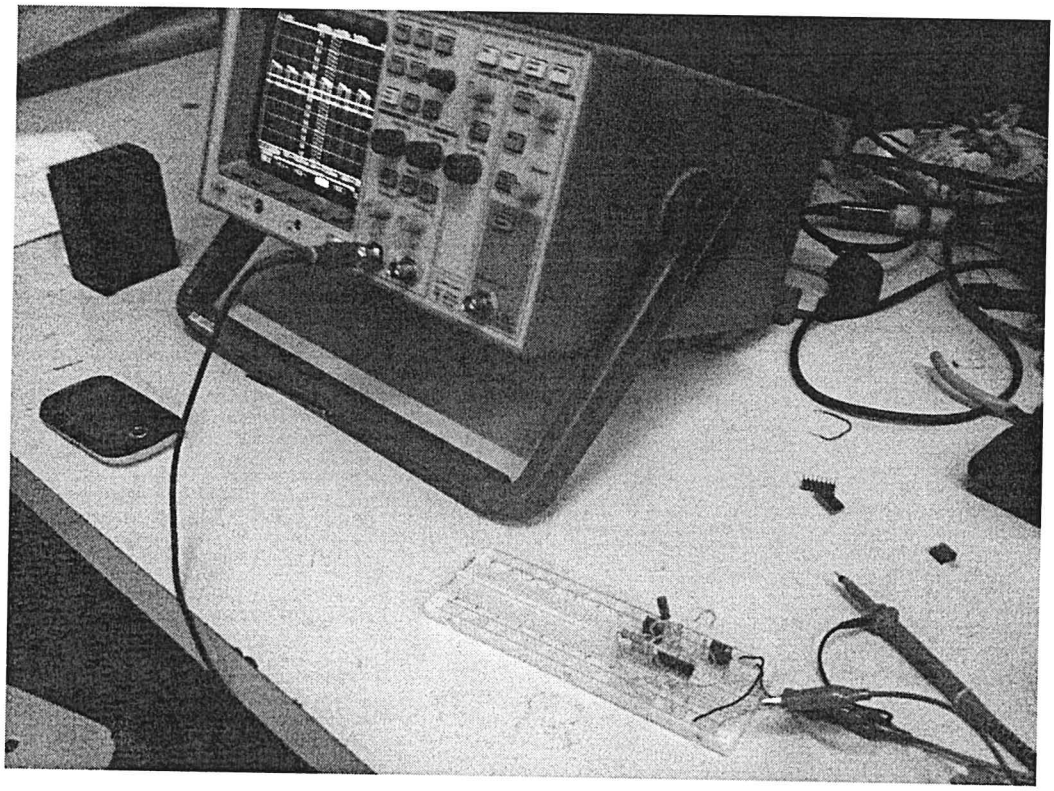


Figure 18. Laboratory test circuit built on breadboard.

Controller circuit is built to the breadboard and the PWM output is obtained. Gate signal is observed by the ossiloscope. Components for the closed-loop operation are also arranged and built. 12V Output voltage is reduced to 6V reference to sent to the reference pin of 3525 for closed loop operation. With adjusting the operating frequency and duty cycle, required values are regulated. Filter inductor which was found on the market was not suitable fort he required parameters. Thus, the inductor was self-constructed again for L=25μH with peak voltage level 12V and the load current 4A at 100kHz frequency.

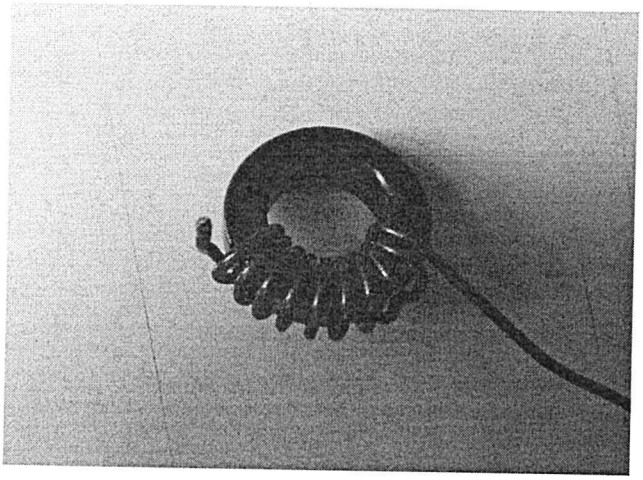


Figure 19. Picture of the inductor during construction.

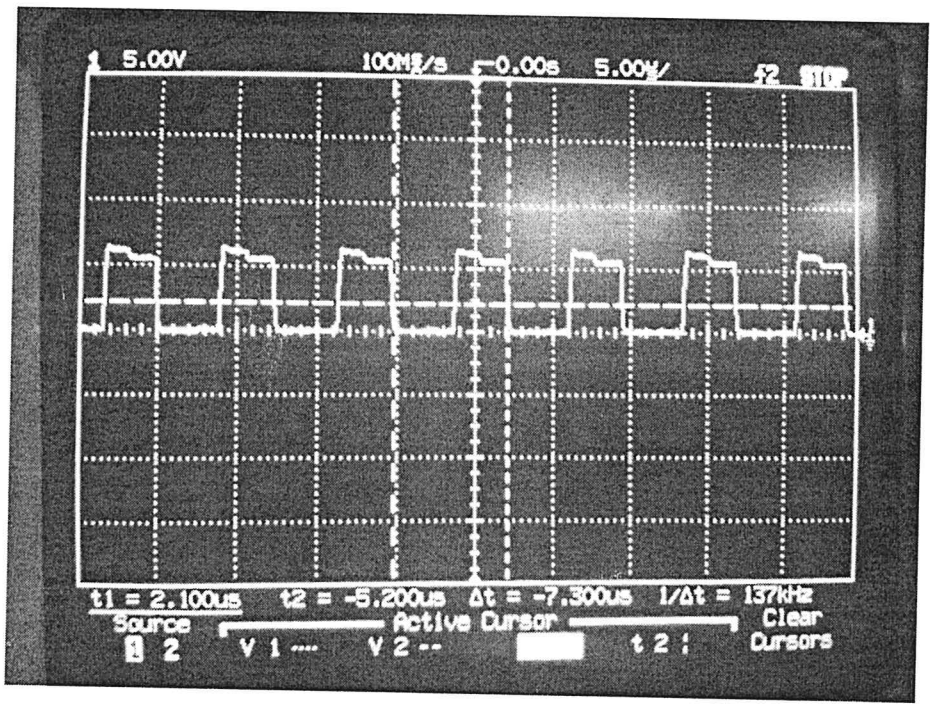


Figure 20. PWM waveform at the output of SG3525 with D=0.5 at frequency f=137kHz.

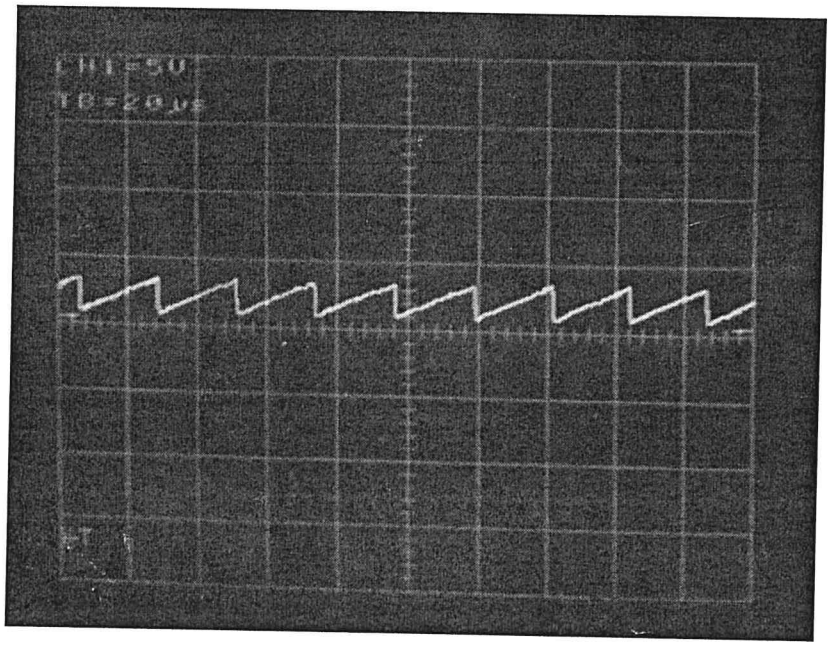


Figure 21. The saw-tooth waveform generated by pin 5 of UC3525 controller chip.

5.2. PCB Layout

After the laboratory testing finished, whole circuit is designed in PROTEUS. PCB Layout is completed in ARES and built on self-constructed board. Higher current flows through the power part. Considering this parameters, tracks for the power stage is thicken. A fuse for input and to protect the load is also take into consideration. Figure .... Shows the PCB layout of the circuit.

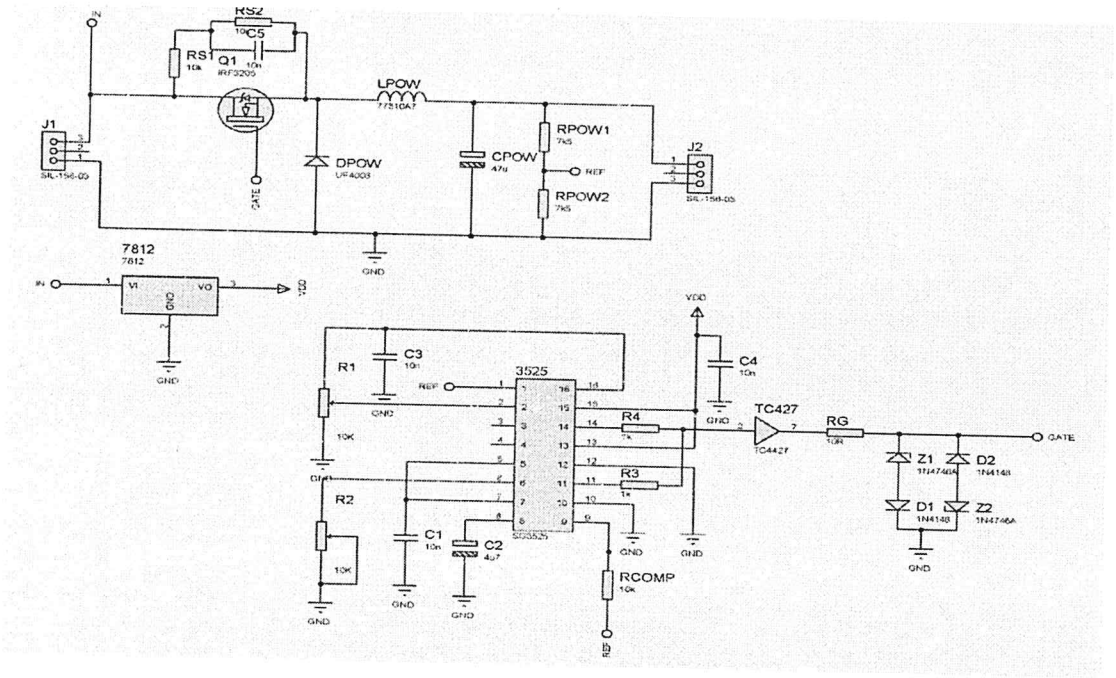


Figure 22. Designed circuit schematic in PROTEUS.

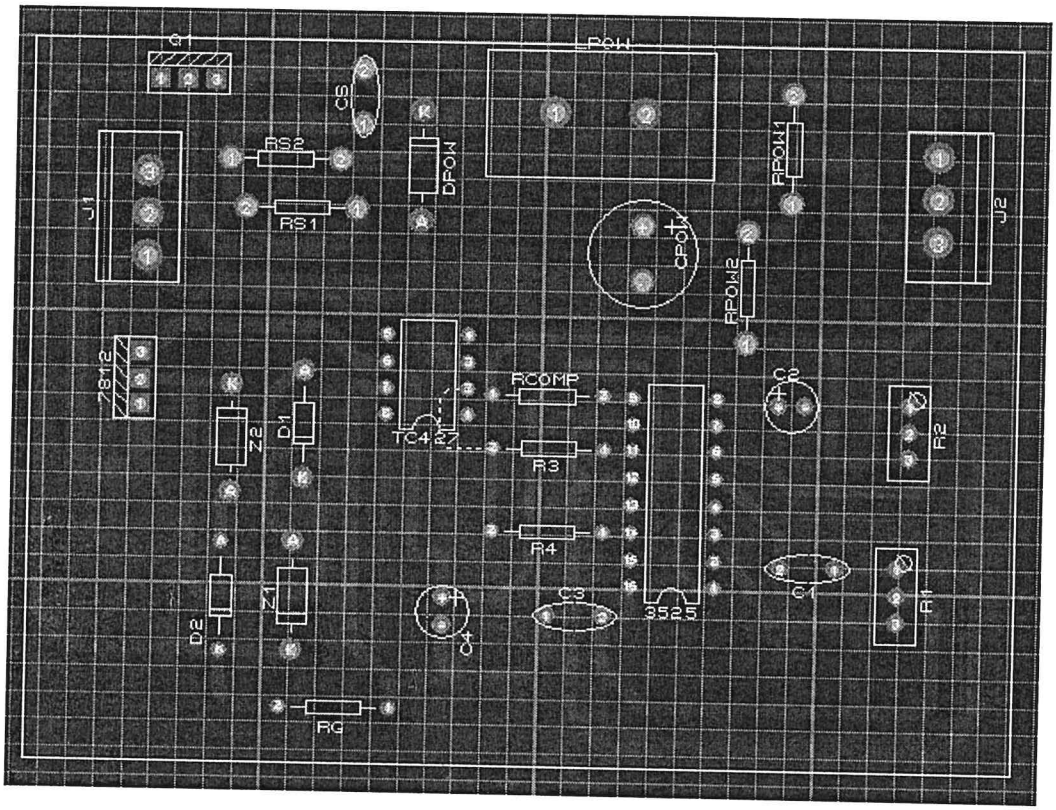


Figure 23. Design of PCB Layout drawn up by the project group in ARES.

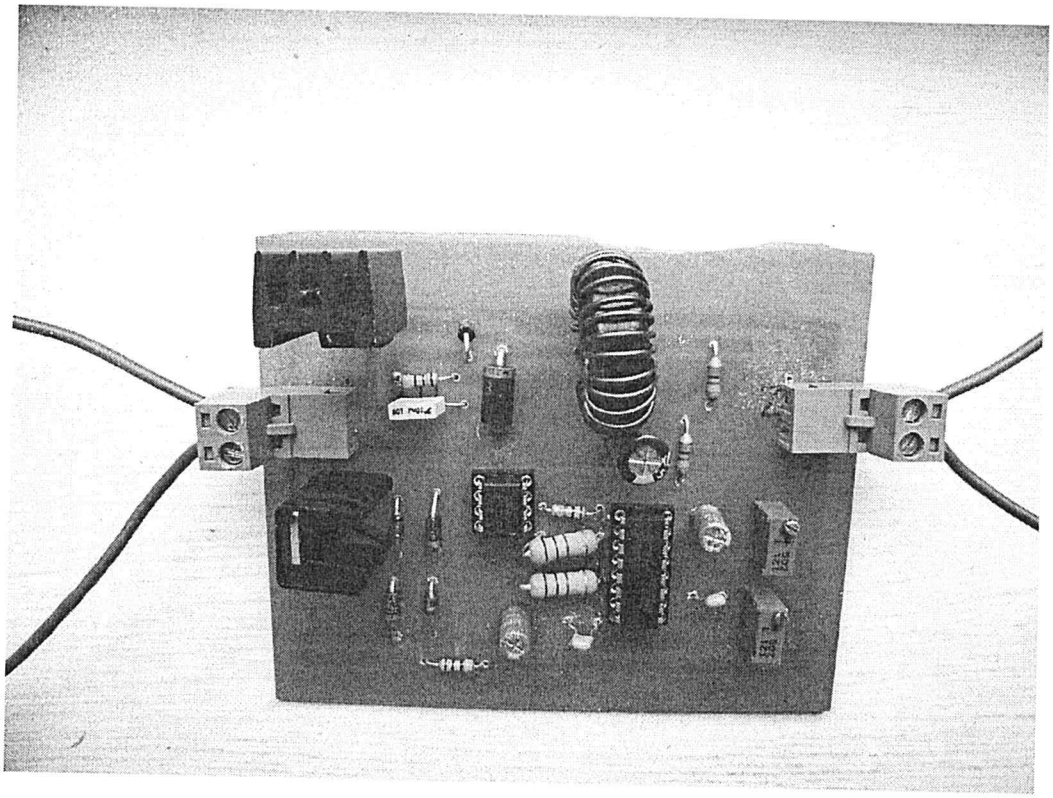


Figure 24. PCB Layout (front).

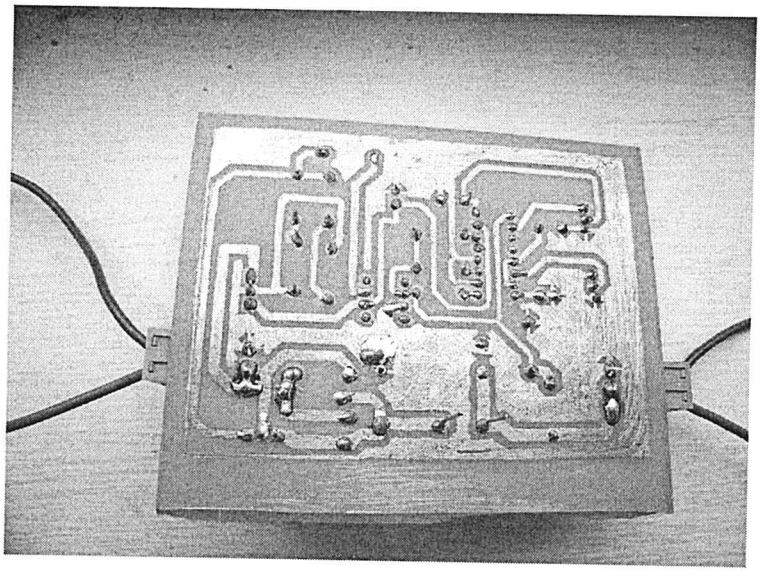


Figure 25. PCB Layout (back).

6. Result and Comments:

Required design and build process on breadboard is completed. Demanded simulation graphics are obtained.

After the interim process, appropriate snubber circuit design and PCB design is completed. After the snubber circuit construction, it is observed that switching losses decreased. Controller and power circuit is built to PCB. Whole circuit is tested with the load and overall required parameters is explained in the project report..

7. Appendix

[1]. PWM Controller: SG3525A Datasheet

[2]. Gate Driver: TC427 Datasheet

[3]. Power MOSFET: IRF3205 Datasheet